REMARKS

Claims 1-42 are pending in the present application.

Claims 1-9, 12-23, 26-36, and 38-42 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hunter et al. (U.S. Patent No. 5,394,555). Applicant respectfully traverses this rejection.

Claims 10, 24, and 37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hunter in view of Farmwald et al. (U.S. Patent No. 5,606,717). Applicant respectfully traverses this rejection.

Claims 11, 25, and 38 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hunter in view of Baxter et al. (U.S. Patent No. 5,887,146), and in further view of Martin et al. ("Bandwidth Adaptive Snooping") (hereinafter "Martin"). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites a system comprising in pertinent part,

> wherein **an active device** included in a node of the plurality of nodes is configured to **initiate a write back transaction** involving a coherency unit **by sending either a first type of address packet or a second type of address packet** on the address network **dependent on whether the active device is included in a multi-node system**. (Emphasis added)

The Examiner asserts Hunter teaches each and every limitation recited in Applicant's claim 1. Applicant respectfully disagrees with the Examiner's characterization of Hunter and the application of Hunter to Applicant's claims. More particularly, the Examiner asserts Hunter teaches the limitations at col. 4, lines 20-25. Applicant disagrees. Specifically, Hunter actually teaches at col. 4, lines 9-25

> The DSBA is an environment which offers the simplest way to understand the real-time operation of SOs. Referring to FIG. 2, each node in the cluster (only two nodes of two CPUs 1 each are shown for simplicity) contains an **External Coherency Unit (ECU)** 10 that: (a) **snoops its own node-local bus 4 for**

> **commands on shared cache-lines that are also present in other nodes**, and (b) **conditionally forwards these commands (using a unique identifier for the cache-line) to the other nodes via, for example, a separate inter-node ECU bus** 11. (Point-to-point connections are also possible, using a directory in each ECU to keep track of which nodes have copies.) All other **ECUs**: (a) snoop the inter-node ECU bus 11 for commands that affect cache-lines resident in their own local memories, (b) translate these to their own physical tags and (c) inject the translated commands into their own node-local buses. (Emphasis added)

From the foregoing, it is clear that Hunter is disclosing the CPU (the active device not the ECU) sending **one type of command** within the node, and the **ECU (interface) within the same node** sends the command with a unique identifier across the ECU bus. An ECU within a different node translates the command into physical tags and then sends the translated commands within the other node based upon snooping traffic on the various internal and external buses. Furthermore the ECU sends the different command dependent upon whther the cache line is present in another node, not whether there is another node present. This is clearly not the same as **a given CPU within in a node** sending on an internal bus one type of address packet (command) if it is in a multinode system, and a different type of address packet if it is not in a multinode system.

Accordingly, Applicant submits Hunter does not teach or disclose "wherein an active device included in a node of the plurality of nodes is configured to initiate a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on the address network dependent on whether the active device is included in a multi-node system," as recited in claim 1.

Regarding the rejection of claim 2, the Examiner asserts hunter teaches the limitations at col. 7, lines 21-24, col. 4, lines 21-25, and col. 6, lines 21-26. Applicant respectfully disagrees. More particularly, Hunter discloses

> All other **ECUs**: (a) snoop the inter-node ECU bus 11 for commands that affect cache-lines resident in their own local memories, (b) translate these to their own physical tags and (c) inject the translated commands into their own node-local buses. (*See* Hunter col. 4, lines 21-25) (Emphasis added)

> For example, if a CPU wishes to obtain an exclusive copy of a shared cache-line, **it places a suitable command** (e.g., **RTW--"read with intent to write"**--in the exemplary system to be explained more fully below) on its node-local bus which will cause each ECU 10 to take the following set of possible actions:
> (1)if the cache-line state is exclusive or modified, it will be retrieved directly from local memory 3 and sent to the requesting processor with no remote action taken because no other copies exist;
> (2) if the state is invalid, an RTW command will be transmitted over the inter-node ECU bus 11 to other nodes. A remote node that contains the line in exclusive or modified state will transmit (siphon) the cache line over the inter-node ECU bus to the requester. If several nodes contain the line in the shared state, all attempt to send it, but ECU bus conventional priority logic will choose one and cancel the others. All remote copies will be set to the invalid state.
> (3) if the state is shared, the INV command will be sent to other nodes, which cause them to set their states to invalid (siphoning is not necessary because a current copy already exists in the requesting node). (*See* Hunter col. 6, lines 21-45) (Emphasis added)
>
> A modified shared page that has not been referenced for some time can evicted by signaling (e.g., **via special interrupt**) the home node to write it to disk 18 (FIG. 3). (*See* Hunter col. 4, lines 21-24) (Emphasis added)

From the above disclosure in Hunter, it is clear that the CPU sends the RTW comand, and the cache line will be retrieved locally, or **the ECU** will send the RTW command to other nodes, or **the ECU** will send an INV command to other nodes. Applicant submits this is in contrast to the CPU (active device) sending an RWB packet in a multinode system or a WB packet in a single node system, and the active devices in the local node changing ownership in response to an RWB packet.

In regard to the rejection of claim 10, the Examiner asserts Hunter teaches the owner of a node providing data about a coherency unit at col. 6, lines 31-40, and acknowledges Hunter does not teach the use of a NACK packet. The Examiner further asserts Farmwald teaches the use of a NACK packet. Applicant respectfully disagrees

with the Examiner's characterization of both Hunter and Farmwald. More particularly, Applicant submits the claim recites far more language than the use of a NACK. Specifically, at col. 31-40 Hunter actually discloses at col. 6, lines 21-40

> For example, if a CPU wishes to obtain **an exclusive copy** of a shared cache-line, it places a suitable command (e.g., RTW--"read with intent to write"--in the exemplary system to be explained more fully below) on its node-local bus which will cause **each ECU 10** to take the following set of possible actions:
> (1) if the cache-line state is exclusive or modified, it will be retrieved directly from local memory 3 and sent to the requesting processor with no remote action taken because no other copies exist;
> (2) if the state is invalid, an RTW command will be transmitted over the inter-node ECU bus 11 to other nodes. A remote node that contains the line in exclusive or modified state will transmit (siphon) the cache line over the inter-node ECU bus to the requester. If several nodes contain the line in the shared state, all attempt to send it, but ECU bus conventional priority logic will choose one and cancel the others. All remote copies will be set to the invalid state. (Emphasis added)

From the foregoing, it is clear Hunter is merely teaching a CPU requesting a cahe line locally, and if the cache line state is exclusive, the cache line is retrieved locally, if the state is invalid, the RTW command is sent by an ECU in the node to other nodes. Another node that owns the line retrieves the data and provides it to the requester. If several nodes have the cache line in the shared state, they may all try to send it but the ECU will choose one and cancel the others.

Farmwald is directed to a memory circuit and merely discloses the use of NACK signalling.

Applicant fails to see how the above disclosure in Hunter and Farmwald teaches "... **if the active device sends the RWB** address packet **and another active device included in the node gains ownership** of the coherency unit **before** an interface included in the node sends a responsive address packet, the other active device is configured to provide data to the interface in response to the responsive address packet;" or "wherein **if** the active device **sends the WB** address packet and **the other active**

device included in the node gains ownership of the coherency unit **before a memory subsystem included in the node sends a different responsive address packet**, the active device is configured to send a **NACK data packet** to the memory subsystem," as recited in claim 10. Applicant contends it does not.

In regard to the rejection of claim 11, neither Martin nor Baxter is relied upon to teach (nor do they teach) the limitations recited in Applicant's claim 1. Applicant submits neither Hunter nor Baxter nor Martin teaches or suggest the combination of features recited in claim 11.

Thus for the reasons given above, Applicant submits claim 1 along with its dependent claims patentably distinguishes over Hunter, and over Hunter in view of Farmwald, and over hunter in view of Baxter and Martin.

Applicant's claims 16 and 28 recite features similar to the features recited in claim 1. Accordingly, Applicant submits claims 16 and 28, along with their respective dependent claims, patentably distinguish over Hunter, and over Hunter in view of Farmwald, and over hunter in view of Baxter and Martin for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-13301/SJC.

Respectfully submitted,

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